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Simple, low-cost technique for photolithographic self-aligned top metal contacts to nanowires and nanotubes

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Abstract
We propose a new simple, low-cost method for providing all-round metal contacts to one-dimensional structures such as carbon nanotubes and nanowires on a transparent substrate. The nanostructures are first positioned in place to bridge a electrode gap by dielectrophoresis. The electrode structure is then used as a self-aligned mask during the subsequent photolithography through illumination from the substrate backside. This is followed by metallization and lift-off. Our measurements on multi-walled carbon nanotubes thus contacted show reasonable yield and good electrical contacts for the process carried out on a glass slide as the substrate.

1. Introduction

Ever since the discovery of the carbon nanotube (CNT) by Ijima [1], many applications have been sought that exploit the electronic properties of various one-dimensional nanostructures (hereafter called NWs) such as CNTs [2], nanowires [3, 4] and nanobelts [5]. These include electronic circuit-based applications such as field-effect transistors, logic circuits, nanoelectromechanical systems, oscillators and interconnects [2–4], and sensing-based applications for gases, chemicals, biomolecules, etc [6, 7].

Even though 17 years have passed since the discovery of CNTs, the fabrication of robust and reliable contacts for electrical measurements remains one of the most difficult and complicated processes for NWs. A survey of various popular techniques for providing electrical contacts to NWs shows none of them to be a truly effective technique [8]. They are plagued by the need for expensive instrumentation, low yield or difficult processes. Top-down metal patterning techniques by lithographic methods are the most commonly used. Electron beam lithography (EBL) followed by metal evaporation on nanostructures dispersed on a non-conductive substrate is the most popular technique, but it requires the use of an EBL system and a highly skilled operator since overlay accuracy is of the utmost importance. Optical lithographic masking techniques are an alternative but the inflexible nature of optical masking quite often requires the nanostructure to be physically placed at the desired location first either by direct manipulation [9], self-assembly [10] or dielectrophoresis (DEP) [11]. The overlay accuracy requirement for smaller nanostructures also requires the use of a highly precise and costly stepper system. Other techniques include nanostenciling by atomic force microscopy (AFM) [12], wire shadow masking [13] and direct wiring by electron-beam-induced deposition EBID [14] or focused-ion beam induced deposition [8].

Alternatively, the NWs can be placed on the electrodes instead. DEP is the most popular, since it is fairly automated and does not require specialized skills and equipment. Other similar techniques include direct manipulation [8, 15] and dispersion on pre-patterned electrodes [8, 16]. However, the electrical measurement results are generally poor and measurements tend to be dominated by contact resistance [15, 16]. This could be attributed to a variety of reasons including poor physical contact, presence of contaminants, metal oxides at the interface and mismatch of Fermi levels. To overcome the issues associated with the contact resistance, a top layer of metal is normally introduced on top of the NW [11]. The sensitivity of electrical contact is such that even an overcoating metal with poor

step coverage on a nanostructure is sufficient to cause poor contact [8]. Alternatively, nanosoldering techniques such as focused-ion-beam or electron-beam-induced deposition of gold, platinum or other metals [8, 15, 16] are also routinely used to improve contact. An alternative is *in situ* nanostructure growth [17–20]. However, the limitation lies in the ability to control the properties of the nanostructure as well as maintain compatibility with the substrate.

For reliable electrical connection with low contact resistance to a nanostructure, the contacting metal should completely envelop the end of the nanostructure. However, the techniques used often require expensive equipment and highly specialized skills. In short, the lack of a simple and reliable way of measuring the electrical characteristics of a nanostructure is an impediment to garnering statistically meaningful results. In this paper, we propose a simple and low-cost self-aligned technique for applying a top metal onto nanostructures after DEP for electrical measurements.

2. Experimental technique

The first part of the process involves fairly conventional techniques for fabricating the electrodes. However, instead of the more usual SiO_2 on silicon, a transparent substrate such as a microscope cover glass or quartz plate is used. A positive photoresist (AZ Photoresist 1512) is spun onto the substrate at 6000 rpm to a thickness of 1.04 μm. Photolithography is carried out using a contact mask and a UV LED (Hero HUVL400-510, peak wavelength 400 nm, biased at 20 mA), that can be easily purchased, as a point light source. AZ Photoresist 1512 was chosen because of its relatively high sensitivity at 400 nm. Exposure time was 4 min at a distance of 10 cm from the LED and the sample was developed in AZ developer. This simple set-up is capable of a resolution of 2 μm, provided the mask and the sample are in good contact. The metal electrodes are formed by evaporating 5 nm Cr and 120 nm Au. It is imperative that the metal layer is thick enough to be opaque for the subsequent processing step. Comparing between a silicon dioxide-on-silicon substrate and a glass substrate, we find that straightforward evaporation results in melting of the resist on the glass substrate. Since glass has a thermal conductivity a hundred times poorer than that of silicon, heat from the condensation of the metal is trapped in the resist, causing it to flow and deform. To minimize this effect, we evaporated Au in steps of 10 nm with a break of 10 min in between, to allow the heat to dissipate. Soaking in toluene prior to photolithography to create an overhang [21] did not help as the overhang eventually deformed during metal evaporation. This is followed by lift-off in acetone and blow-drying in N_2. This process quite often resulted in the formation of crowns around the electrode due to tearing of the metal during metal lift-off. To reduce the crowns on the electrodes, the sample is placed in a high powered ultrasonic bath for about 10 min to break off the crowns.

In this particular example, we have chosen to use arc-discharge multi-walled carbon nanotubes (MWNT) from MER Corporation with a diameter of 6–20 nm and lengths of about 1–5 μm as the nanostructure under test. The MWNTs

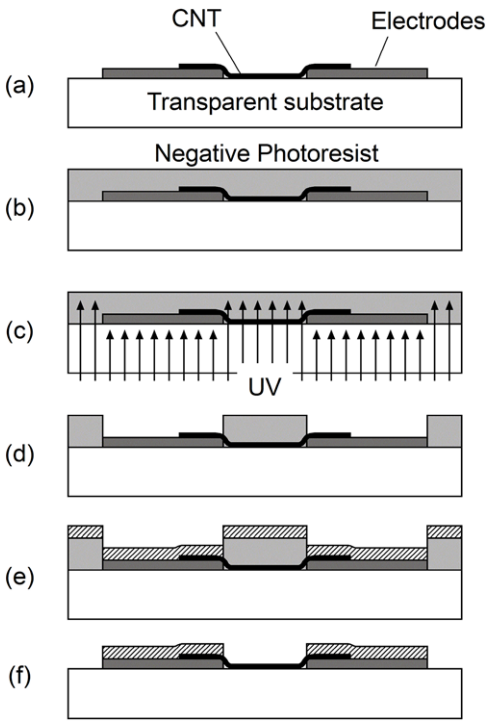

Figure 1. Processing steps for the sample after DEP.

were dispersed in dimethylformamide (DMF) using a SONICS ultrasonic processor for 30 min. DEP was used to place the MWNTs on the electrode, using a probe station and a signal generator (Thandar TG2001) at a frequency of 1 MHz and an AC voltage of 3 $V_{p\text{-}p}$ superimposed on a DC voltage of 0.3 V (figure 1(a)). The concentration of the MWNT was optimized for approximately 5–20 MWNTs across the electrodes.

The sample was spin-coated with a negative resist (ma-N 1407 from Micro Resist Technology) (figure 1(b)) at 3000 rpm to a thickness of 700 nm. Care should be taken to prevent the resist from going under the sample. The presence of resist on the bottom of the sample can affect the exposure in subsequent steps. The sample was then flipped over and exposed from the substrate side using the same LED as used for the front-side lithography of the electrodes (figure 1(c)). Since the substrate is transparent to near-UV light, the resist was exposed to the UV light. However, the resist on the electrodes was masked by the electrodes and remained unexposed. The distance from LED to sample was 4.5 cm and exposure was carried out for 500 s. The sample was placed on a small aperture on a box with the inside coloured black to reduce light reflections from surfaces below the sample. Overexposure can cause carbonaceous residue to form on the glass, since exposure is from below. Significant overexposure can cause the resist to harden and result in difficult removal later. The sample was then developed for 30 s (Micro Resist technology ma-D-533/S) (figure 1(d)). We deliberately overdeveloped the resist to ensure there was no residue left on the electrodes. On the other hand, under-exposure and/or overdevelopment will result in the resist having a sloping profile and may result in difficulty during metal lift-off. This self-masking process resulted in photoresist covering the MWNTs in between the

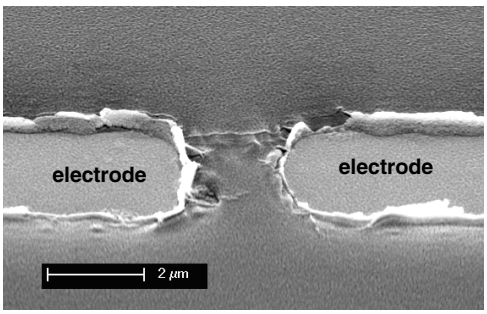

Figure 2. After second layer metal deposition, photoresist masks the gap and the rest of the die except for the electrode.

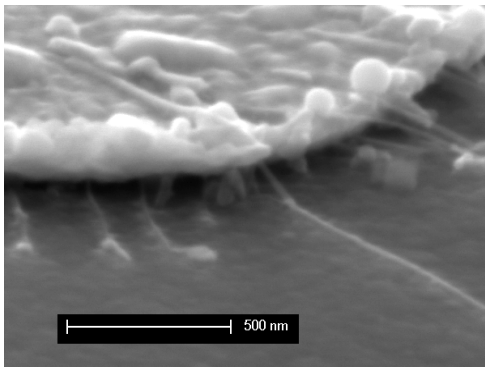

Figure 3. CNT sandwiched between the top metal and bottom electrode after second layer metal deposition and lift-off. Substrate SiO_2 on ITO-coated glass.

electrodes as well as the rest of the sample but not on the electrodes. A second layer of metal of 8 nm Ti and 20 nm Au was subsequently evaporated on the sample, as shown in figures 1(e) and 2. A physical shadow mask can be placed on the sample exposing only the relevant area and masking other critical features such as bond pads, etc, before evaporation. This was followed by a lift-off process in acetone (figure 1(f)). A slight ultrasound agitation is normally necessary for the second metal layer to lift off. The sample was then rinsed in IPA and blown dry in N_2. The result is shown in figure 3. The sample was then annealed in a tube furnace in an argon ambience at 420 °C for 8 min (5 min ramp, 3 min anneal) to improve the metal contact. The furnace is rapidly cooled by forced convection after annealing.

An alternative substrate would be the use of indium–tin oxide (ITO)-coated glass that has been covered with an additional layer of SiO_2. The ITO layer would allow backgating of the nanostructure. The use of this substrate would also reduce charging and allow better imaging in an SEM. However, care must be taken to prevent the formation of pinholes in the SiO_2 layer.

3. Yield analysis

For this experiment, two-point electrical measurements were taken after DEP using a probe station and a Keithley 4200 parameter analyser with a sweep of ±1 V and a current

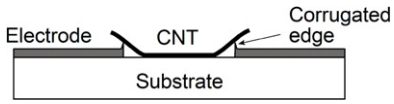

Figure 4. Side view of a CNT/NW in between two electrodes.

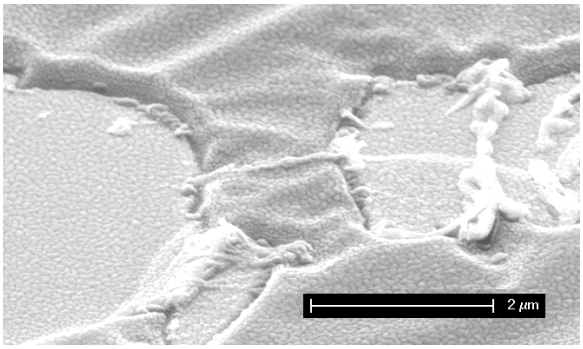

Figure 5. SEM image of an electrode with MWNT after second layer metal deposition with a continuous film.

compliance of 100 μA. This was repeated after the second metal deposition and after annealing. For yield analysis of the processes involved, 10 dies of glass slide coverslips with six sets of electrodes each are considered. Yield is considered at three stages: after DEP, after the second layer metal, and after annealing. This amounts to 60 sets of electrodes for two-point measurement. After DEP, 51 sets of electrodes (85%) show electrical conduction (<100 MΩ). The electrical yield after the second layer metal process is 28 sets (55%). Our experience shows there is a lot of variance in the yield for this process. We believe the evaporation of the second layer metal on the negative photoresist causes some melting of the resist and results in 'blunting' of the sharp edges of the resist profile. Unfortunately this causes the metallic film to be continuous (figure 5) and results in an electrical short across the electrode or tearing of the second layer metal film on the electrode during metal lift-off. We find that increasing the negative-resist exposure to the UV reduces this yield loss but at the expense of increased carbonaceous residue after annealing of the sample. There are also instances where the electrodes do not appear to have any physical defect but show no conduction after the second metal layer. In such cases we believe the MWNTs have been swept off or torn away during the metal lift-off process. The resistance of all the electrodes did not necessarily decrease compared to prior to the metal deposition process. In such cases we believe that some, if not all, MWNTs have been swept off or torn away during the metal lift-off process. Annealing the sample improves conductivity generally but causes two sets of electrodes (7%) to cease being conducting. We believe it is caused by thermal expansion/deformation of the local geometries of the electrode. For statistical reasons we classify the electrode to be electrically yielding if the resistance is less than 200 kΩ at 1 V, in which case our overall yield is 24 sets of electrodes (40%). Only two sets of electrodes show resistance between 200 kΩ and 2 MΩ. The rest of the samples were either torn or electrically shorting.

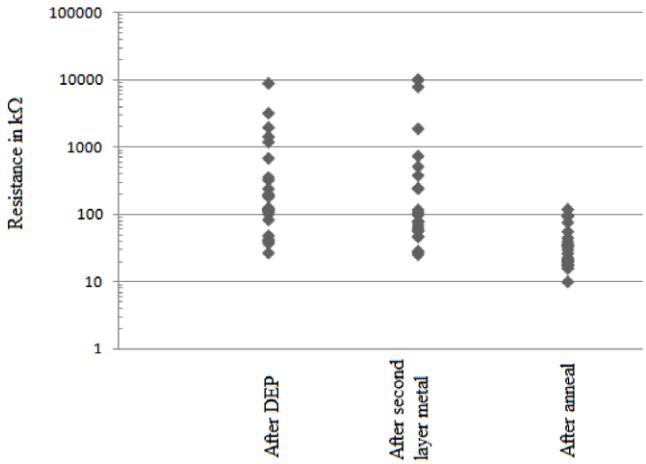

Figure 6. Scatter plot of the resistance measurement for the 24 electrodes at various stages.

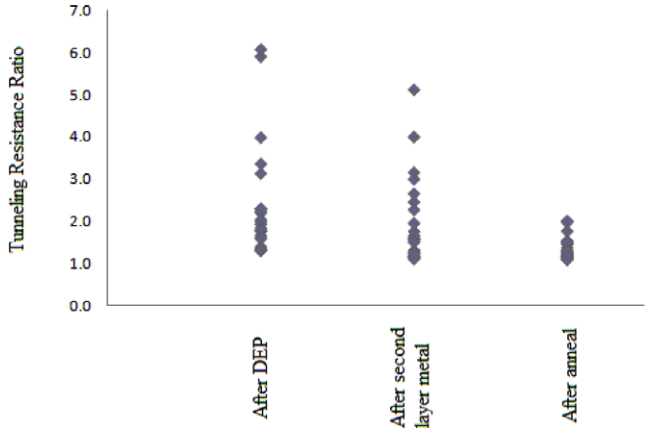

Figure 7. Scatter plot of the tunnelling resistance ratio for the 24 electrodes at various stages.

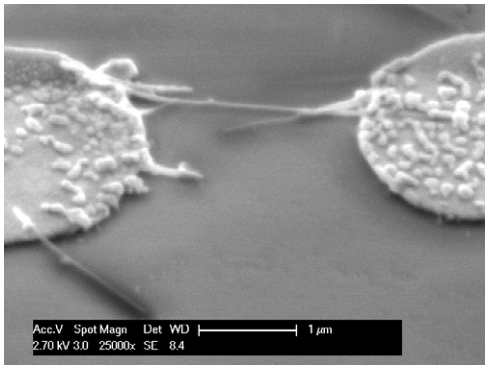

Figure 8. SEM micrograph of a single MWNT across the two electrodes. Imaging was done at 2.7 keV with the electrodes grounded by carbon tape, at a tilt angle of 45° to reduce charging of the substrate during viewing.

4. Results and discussion

The overall resistance of the structure can be considered as a combination of the ohmic resistance and the tunnelling resistance. The ohmic content is constant at all voltages, whereas tunnelling resistance is dependent on the voltage. As an indication for the tunnelling component of the series resistance, the resistance at 1 V ($R_{1\ \mathrm{V}}$) and at 100 mV ($R_{100\ \mathrm{mV}}$) is compared. The resistance of the 1 V and the ratio of resistance ($R_{100\ \mathrm{mV}}/R_{1\ \mathrm{V}}$) (hereafter called tunnelling resistance ratio) of the 24 yielding electrode pairs were compared at the three stages as in the yield analysis.

The resistances after DEP showed large variance and were anywhere between a few tens of kΩ to a few tens of MΩ (figure 6). Some were nonlinear, showing tunnelling behaviour with much higher resistance at low voltages and generally had poor measurement repeatability. There is also a very large variance in tunnelling resistance ratio with values between 1.3 and 6.1 (figure 7). We believe the large variances are due to the local geometry of the contact between the MWNTs and the electrode. Figure 1(a) represents an idealized figure of the placement of a nanostructure on electrodes. In reality, a closer representation is shown in figure 4. Although with slow evaporation melting of the resist is minimized, the profile of the resist is still poor. With poor resist profile control (no undercut), metal lift-off for electrode fabrication tends to leave some corrugated edges where the metal tears off. The use of the ultrasonic bath mitigates the condition slightly but does not eliminate it completely. This results in point contact for some MWNTs and hence the high contact resistance. A large overlap between the MWNT and the electrodes would reduce the contact resistance. Tunnelling resistance ratio improved slightly after the second metal deposition with 70% of the electrodes having a ratio of less than 2 compared to only 54% after DEP. The actual distribution of resistances itself did not change that much, for reasons described in the previous section. Annealing the samples caused the resistance of 80% of the samples to decrease further to a few tens of kΩ, consistent with most studies of MWNTs [8, 15, 16, 22]. Linearity improved significantly showing near-ohmic behaviour with 80% of the samples having tunnelling resistance ratios of less than 1.5 (figure 7). Our studies show that the resistance of the MWNT–electrode system is highly dependent on the annealing conditions. A brief high temperature (>400 °C for a few minutes) anneal tends to give lower resistances. A long anneal at lower temperature (300 °C for an hour) can actually result in higher resistance than the as-deposited second metal layer. Scanning electron microscope (SEM) examination of the samples shows the electrode pairs with very low resistance (<20 kΩ) tend to have an MWNT with a large overlap with the electrodes. Samples with more than one MWNT with a large overlap are rare since the MWNTs are around 1–5 μm in length and the gap is around 2–3 μm. Since the overall resistance is now low enough to allow for high current flow at low voltages, we find that forcing a high current through (>100 μA) after annealing can quite often improve the contact resistance further.

An example of the various stages of the evolution of the contact to an MWNT (figure 8) is shown by the I–V and resistance plots in figure 9. As deposited by DEP, the MWNT showed non-ohmic contact and had a circuit resistance of about 10 MΩ at 2 V, which increased fivefold at 1 V. At very low

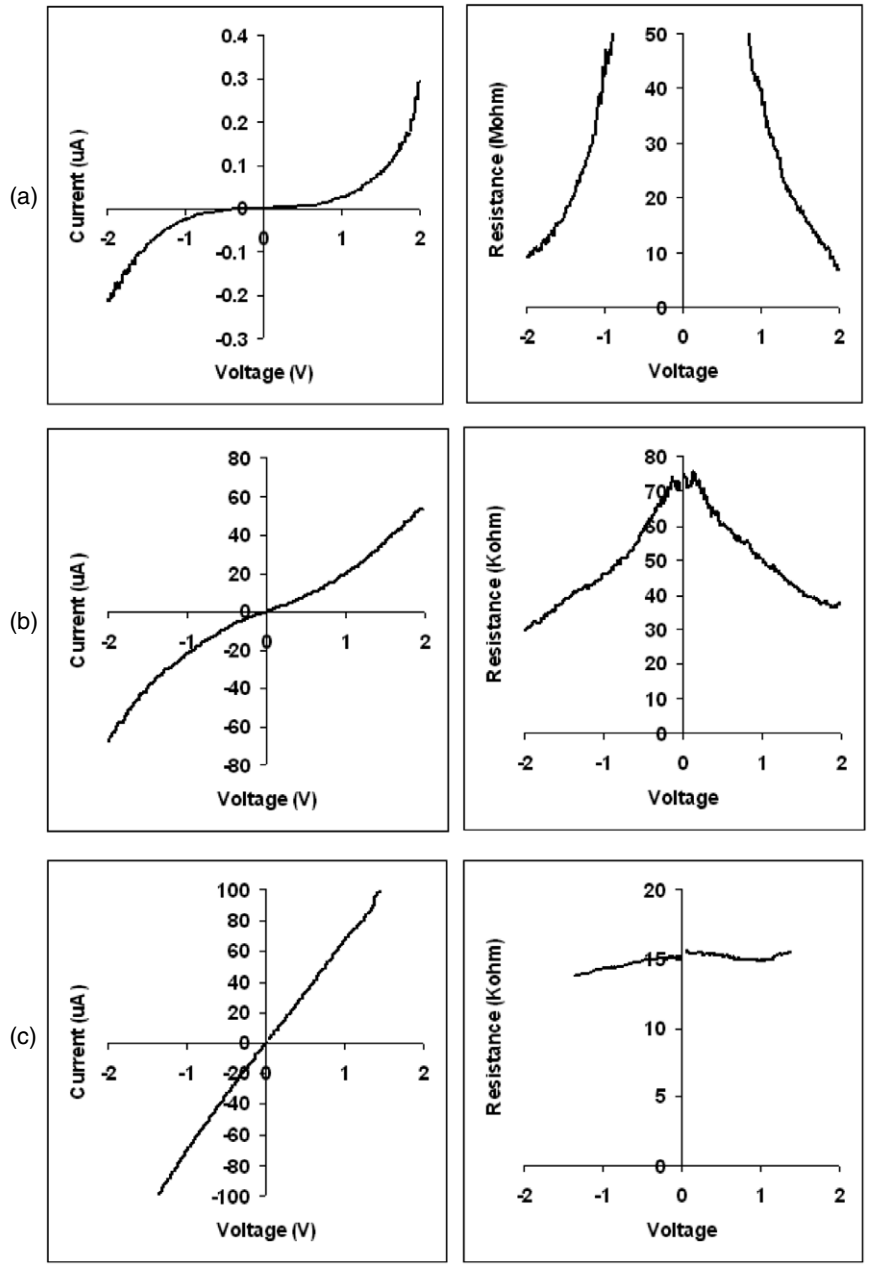

Figure 9. I–V characteristics of a single MWNT across the electrodes at various stages of the process. The measurement was done at ±2 V to better illustrate the evolution of the contact resistance.

voltages, the MWNT was essentially non-conducting. Non-conductance of a single MWNT even though there is physical contact with an Au electrode is quite commonly observed prior to nanosoldering [15, 16]. After application of the second layer metal, the contact resistance improved significantly and the measured resistance of the structure was then about 30 kΩ, increasing to 70 kΩ at low voltages. After annealing the structure, the resistance reduced even further to about 15 kΩ, approaching its theoretical value of 12.9 kΩ [23]. Linearity improved with each step, with the sample showing near-ohmic behaviour after annealing. The current density at 100 μA would be $\sim 3 \times 10^{11}$ A m^{-2} (assuming the MWNT has a diameter of 20 nm).

5. Conclusion

The self-aligned technique is capable of placing a top layer of metal on existing electrodes consistently and reliably. The technique is versatile and can be optimized for a variety of nanostructures by varying the material and thickness of the top metal layer. The nature of this process allows for the fabrication of a large number of samples with reasonable yield. The electrodes could alternatively be connected along the scribe line, allowing for parallel DEP for wafer-scale processing. The connection would be severed during singulation of the die from the wafer. The simplicity and low-cost nature of this technique makes it a potential candidate for lab-on-a-chip manufacturing. Yield loss is mostly from

second layer metal lift-off resulting in a continuous metal film. Yield loss of this nature could be reduced by the use of a more thermally conductive substrate such as quartz or sapphire and optimizing the process. Annealing of the contacts is very crucial and should ideally be performed by rapid thermal annealing rather than the use of a tube furnace.

The resistance measurements of a few tens of kΩ that we obtained are similar to those achieved using EBL and other techniques. However, three-dimensional topographies, such as crowns, steps and overlaps around the area of the contacts, play a role in the quality of the contact. Although we had used this technique for two-point measurement, four-point measurement with top metal is also possible, provided the nanostructure is able to bridge all four bottom contacts.

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